ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit having a system bus divided into stages and configured to transfer signals, stage elements configured to connect the stages in series and operate in a divided mode transferring signals from a stage on an input side to a stage on an output side in synchronization with a clock signal and in a through mode that always passes signals from the stage on the input side to the stage on the output side, and a plurality of function modules connected to the different stages.